L Number	Hits	Search Text	DB	Time stamp
1	8	(data with retention with lifetime) and (ferroelectric with memorY)	USPAT; US-PGPUB	2004/07/23 09:50
2	5	(data with retention with lifetime) and (ferroelectric) and temperature	USPAT; US-PGPUB	2004/07/23 09:52
3	19	(data with retention with lifetime) and memory and temperature	USPAT; US-PGPUB	2004/07/23 10:02
4	19	((data with retention with lifetime) and memory and temperature) and @ad<20030624	USPAT; US-PGPUB	2004/07/23 09:53
5	2	(data with retention with lifetime) and memory and temperature	EPO; JPO; DERWENT; IBM TDB	2004/07/23 10:02

US-PAT-NO: 6687648

DOCUMENT-IDENTIFIER: US 6687648 B1

TITLE: Method of predicting reliabilty of oxide-nitride-oxide based non-volatile memory

---------- KWIC ---------

Brief Summary Text - BSTX (4):

Silicon Nitride based Non-Volatile Memory has many advantage as compared to its floating gate and tunneling oxide based counterparts. Silicon-Oxide-Nitride-Oxide-Semiconductor (SONOS) is potentially very dense in terms of number of cells per unit area that can be used and it requires fewer process steps as compared to the floating gate memory. Moreover, it can be easily integrated with the standard SRAM technology. The other advantages of using SONOS devices include their suitability for applications requiring large **temperature** variations and radiation hardening. There has been much apprehension in using SONOS on a wide scale in the industry because the behavior of SONOS with respect to data retention and endurance has been found unpredictable especially with variations in **temperature**.

Brief Summary Text - BSTX (5):

There is a need for an understanding of the physical mechanism and a working model to predict the behavior of SONOS in order to reap the benefits of this technology. Attempts have been made in the past to model the physical mechanism of data retention at high temperatures. Miller, McWhorter, Dellin and Zimmermann (Journal of Applied Physics 67(11), Jun. 1, 1990, pp 7115-7124)

have studied in detail the performance of "Excess Electron" states and "Excess Hole" states and their differences. The data used for this study is taken from a transistor device. A significant difference is behavior has been shown between the "Excess Electron" and "Excess hole" threshold states when the programming **temperature** is different from the storage **temperature** and the storage **temperature** is varied.

Brief Summary Text - BSTX (6):

Other studies have led to conflicting conclusions. A study by Ross, Goodman and Duffy (RCA rev. 31,467-1970) showed that the threshold voltage decay rate of Metal-Nitride-Oxide-Silicon (MNOS) transistors was insensitive to temperatures for temperatures up to 125 degrees C. A study on NMOS transistor cycling endurance with **temperature** variations by Neugebauer and Burgess (Journal of Applied Physics 47,3182-1976) suggested that while charge injection for both threshold states (Excess Electron and Excess Holes) was **temperature** dependent, the decay rate of only the excess hole state was increased by elevating the **temperature**. They also found that the programming **temperature,** relative to the storage **temperature** affected the subsequent decay rate. Williams and Beguwala (IEEE Transactions on Electron Devices ED-25, 1019-1978) have found that the decay rate of only the excess electron state of MNOS transistors was **temperature** dependent.

Brief Summary Text - BSTX (9):

While all the work done in the past explains some portion of the SONOS memory program and erase mechanism, there is a need for an explanation of the behavior of SONOS memory over the entire range of **temperature** (e.g., the

industrial **temperature** range) and a lifetime of program-erase cycles. The advantage of having such a prediction of data retention is that reliable products could be produced at a cost advantage compared to other types of non-volatile memories.

Brief Summary Text - BSTX (12):

A purpose of this invention is to provide a tool and a complete process to predict the life of a SONOS Non Volatile Memory element with respect to data retention at various temperatures. This invention provides relationship which utilizes the bake **temperature** and initial threshold margin (difference between the program threshold and the erase threshold) as input and produces the predicted time taken to reach the final threshold margin as the output. A calculation of constants is required which involves a few data points on threshold voltage margin, time and **temperature** as input when the model is used for a new process. The model allows yield improvement and shortens test times. The model permits the estimation of data retention life in the field based on simple test data collected in well-known procedures.

Brief Summary Text - BSTX (15):

This is a first time invention of a model to predict the **retention lifetime for data** stored in a SONOS structure. Previous calculations have all tried to determine the distribution of charge storage or trapping sites, which is difficult to predict in a chemical vapor deposition deposited nitride and hard to calculate. This method circumvents this problem by calculating the change in the height of the oxide potential barrier which is dependent upon the decayed charge. Previously attempted methods have a strong dependence upon the

quality of nitride and estimation of the location of "emission frontier" and
therefore do not provide good results over the entire range of temperatures and
quality of nitride. There is no standardized method to do this calculation.

Drawing Description Text - DRTX (10):
FIG. 9 shows a graph of correlation between the **temperature** and the
threshold voltage for programming, according to an embodiment of the present
invention.

Drawing Description Text - DRTX (11):
FIG. 10 is a graph of a typical rise in erase threshold voltage with
temperature, as obtained from experimental results.

Detailed Description Text - DETX (16):
where t is the total time the programming voltage is applied to the gate, m
is the electron mass; "a" is the thickness of the oxide, which is the width of
the potential barrier, E is the applied electric field, which is simply the
voltage divided by the thickness of the oxide, "q" is the electric charge and
h-bar is Planck's constant divided by 2.pi.. The amount of inversion charge
may be dependent upon **temperature**.

Detailed Description Text - DETX (21):
As discussed above, this model assumes the programming may be done by
injection of charge by Fowler-Nordheim tunneling due to bending of the oxide
conduction band and also direct tunneling of the channel electrons through the
tunnel oxide. The storage element is nitride (traps in the nitride are either
at the interface of nitride with the tunnel oxide or at a certain depth in
nitride). The depth inside nitride is not very important

as long as the
correct effective activation energy is known.
Fowler-Nordheim tunneling has
very little **temperature** dependence. However the channel
carrier density has
temperature dependence and the **temperature** dependence of
programming voltage is
due to the direct tunneling of channel carriers through the
tunnel oxide into
the nitride.

Detailed Description Text - DETX (22):
The erase operation on the other hand is assumed to be
due to the direct
tunneling (through the tunnel oxide) of the electrons
trapped in the nitride
(Frenkel-Poole emission) to the substrate, which is under
accumulation during
erase operation. Frenkel-Poole emission is a **temperature**
dependent mechanism
and therefore the **temperature** dependence of erase operation
comes from the
temperature dependence of the Frenkel-Poole emission.

Detailed Description Text - DETX (25):
Endurance cycling starts two competing processes-charge
storage by
accumulated remnant charges in the nitride and the decay of
charge by the erase
mechanism. At elevated **temperature** the decay is fast and
at lower temperatures
the decay process is slow. At high **temperature** however,
the channel current is
high too and the programming may store more charge than at
lower temperatures.
Therefore the resultant threshold voltage-endurance cycling
curve at high and
low temperatures may not be monotonic. This will be
demonstrated later in this
application with experimental data.

Detailed Description Text - DETX (32):
Using this relationship, according to an embodiment of
the present
invention, a near perfect fit is obtained with the

experimental data. Where
`t` is the data retention bake time, T is the **temperature,** K is the Boltzmann
constant and "Margin" is the difference between write and erase thresholds.
The terms .alpha., .beta. and .UPSILON. are constants.

Detailed Description Text - DETX (45):
It is appreciated that the time scale is logarithmic, which has resulted in
the disappearance of smaller differences between the model prediction and the
experimental data. However the model, to a good extent provides prediction of
the **data retention lifetime** of the device.

Detailed Description Text - DETX (47):
FIG. 9 shows a correlation 90 between the **temperature** and the threshold
voltage for programming. This calculation is based on some assumptions about
the channel doping density and the initial threshold voltage. The graph 90
shows a rapid decrease in the threshold voltage in the beginning followed by a
semi-saturation or gradual decrease. This is a prediction from the model and
matches the experimentally obtained data closely.

Detailed Description Text - DETX (48):
As the **temperature** increases the number of electrons in the channel
increases too. Because of that, there are more electrons available to tunnel
through the tunnel oxide into the nitride. As a result of this, more charge is
stored in the nitride during programming, bringing the threshold voltage down.

Detailed Description Text - DETX (49):
With **temperature** going up the minimum erase voltage is predicted to first go
up and then almost stabilize with very gradual downward trend. FIG. 10

represents a graph 100 illustrating typical rise in erase threshold voltage
with **temperature**.

Detailed Description Text - DETX (52):
This data demonstrated that an erase process has more **temperature** dependency
than the program process, which aligns with Frenkel-Poole emission idea because
Frenkel-Poole emission is **temperature** dependent.

Detailed Description Text - DETX (53):
With an increase in **temperature,** the Frenkel-Poole emission increases and
the rate of charge decay goes up.

Detailed Description Text - DETX (59):
FIG. 13 shows a graph 130 of the minimum voltage required for erasure with
respect to the number of program erase cycles at room **temperature** and a 1.98 mV
pulse.

Detailed Description Text - DETX (60):
FIG. 14 shows a graph 140 of the minimum voltage required for erasure with
respect to the number of program erase cycles at room **temperature** and a 2.76 mV
pulse.

Detailed Description Text - DETX (61):
FIG. 15 shows a graph 150 of the minimum voltage required for erasure with
respect to the number of program erase cycles at room **temperature** and a 5.36 mV
pulse.

Detailed Description Text - DETX (66):
Erasing is a combination of Frenkel-Poole emission and direct tunneling
through the oxide. Frenkel-Poole emission increases with increase in the erase

voltage and also increase in **temperature**. However tunneling through the oxide is dependent upon the oxide potential barrier in such a way that an increase in the size of the potential barrier may increase or decrease the minimum voltage required based on the difference between the oxide potential barrier and the applied voltage.

Detailed Description Text - DETX (67):

This may be seen by examining the tunneling relationship given earlier. This explains why at low pulse widths (which deposit lower amount of charge in the nitride) the minimum voltage first decreases and then increases. The decrease happens when the applied voltage is close to the potential barrier between nitride and oxide. One finding from the model is that at low **temperature,** larger pulse widths are needed for erase or program.

Detailed Description Text - DETX (69):

FIG. 19 is a plot 190 that shows the variation of minimum erase voltage with program-erase cycling at zero degrees C. As the **temperature** goes down, the pulse width has to be larger. This can be seen from the model as well.

Detailed Description Text - DETX (73):

In step 2030, the programmed memory devices may be baked at a first **temperature,** for example 100 degrees C. During the baking period, margin measurements may be made at a variety of time intervals, for example, at 24 hours, 48 hours and 168 hours. It is appreciated that other intervals are well suited to embodiments of the present invention.

Detailed Description Text - DETX (74):

In step 2040, process step 2030 may be repeated for a different baking
temperature, for example 300 degrees C.

Claims Text - CLTX (3):
3. The method as described in claim 2 further comprising: c) programming
said non-volatile memory; d) measuring threshold margin and field E required
for said programming; e) baking said memory at a first **temperature**; f)
measuring threshold margin after the completion of said e); g) baking said
memory at a second **temperature**; and h) measuring threshold margin after the
completion of said g).

Claims Text - CLTX (4):
4. The method as described in claim 3 wherein said first **temperature** is
substantially similar to 100 degrees C.

Claims Text - CLTX (5):
5. The method as described in claim 3 wherein said second **temperature** is
substantially similar to 300 degrees C.

Claims Text - CLTX (10):
10. The method as described in claim 9 further comprising: c) programming
said non-volatile memory; d) measuring threshold margin and field E required
for said programming; e) baking said memory at a first **temperature**; f)
measuring threshold margin after the completion of said e); g) baking said
memory at a second **temperature**; and h) measuring threshold margin after the
completion of said g).

Claims Text - CLTX (11):
11. The method as described in claim 10 wherein said first **temperature** is

substantially similar to 100 degrees C.

Claims Text - CLTX (12):
12. The method as described in claim 10 wherein said second **temperature** is substantially similar to 300 degrees C.

Claims Text - CLTX (17):
17. The method as described in claim 15 further comprising: c) programming said non-volatile memory; d) measuring threshold margin and field E required for said programming; e) baking said memory at a first **temperature**; f) measuring threshold margin after the completion of said e); g) baking said memory at a second **temperature**; and h) measuring threshold margin after the completion of said g).

Claims Text - CLTX (18):
18. The method as described in claim 17 wherein said first **temperature** is substantially similar to 100 degrees C.

Claims Text - CLTX (19):
19. The method as described in claim 17 wherein said second **temperature** is substantially similar to 300 degrees C.

Claims Text - CLTX (22):
22. The method as described in claim 20 further comprising: d) programming said non-volatile memory; e) measuring threshold margin and field E required for said programming; f) baking said memory at a first **temperature**; g) measuring threshold margin after the completion of said f); h) baking said memory at a second **temperature**; and i) measuring threshold margin after the completion of said h).

Claims Text - CLTX (23):
23. The method as described in claim 20 wherein said first **temperature** is substantially similar to 100 degrees C.

Claims Text - CLTX (24):
24. The method as described in claim 20 wherein said second **temperature** is substantially similar to 300 degrees C.

US-PAT-NO: 6339557

DOCUMENT-IDENTIFIER: US 6339557 B1

TITLE: Charge retention lifetime evaluation method for nonvolatile semiconductor memory

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Brief Summary Text - BSTX (12):
This type of nonvolatile semiconductor memory is evaluated by reliability tests. One such test is a charge retention lifetime evaluation test (memory holding time test). A flash memory is, for instance, required to have high charge retention characteristics of more than 10 years at 125.degree. C. Therefore, evaluating the charge retention lifetime requires a long time even at a development stage, and a very high evaluation ambient **temperature** accelerates the evaluation speed.

Brief Summary Text - BSTX (13):
However, there is a case where the evaluation ambient **temperature** cannot be set so high. In addition, when the charge retention lifetime is evaluated at approximately 250.degree. C. or more after rewriting, damage caused to the tunnel film (film 23 in FIG. 9) by rewriting is recovered to prevent the charge retention lifetime from being evaluated accurately. That is, the accelerated heating accompanied by the recovery of tunnel film damage is not preferable for charge retention lifetime evaluation purposes.

Brief Summary Text - BSTX (15):
The present invention has been made in view of the above

problems. A first object of the present invention is to provide a method for evaluating a charge retention lifetime of a nonvolatile semiconductor memory for a short time regardless of an evaluation ambient **temperature**. A second object of the present invention is to provide a method for evaluating a charge retention lifetime of a nonvolatile semiconductor memory for a short time accurately.

Brief Summary Text - BSTX (19):

The charge **retention lifetime** can be evaluated in a **temperature** range at which damage generated in the tunnel film for writing **data** is not recovered. Accordingly, the charge retention lifetime can be evaluated for a short time accurately.

Brief Summary Text - BSTX (20):

The charge retention lifetime can be evaluated in an operational **temperature** range at which the nonvolatile semiconductor memory is used in practice. Accordingly, the charge retention lifetime can be evaluated for a short time accurately. In this case, it is more preferable for a practical use to apply the voltage to the tunnel film at the maximum **temperature** in the operational **temperature** range.

Detailed Description Text - DETX (8):

Next, a charge retention lifetime evaluation method for the flash memory constructed as above is explained. In the present embodiment, after performing a rewriting operation 100 times, a charge retention lifetime evaluation (test) is performed at an ambient **temperature** at which the damage caused to the tunnel film 5 by the rewriting operation is not eased. In this evaluation (test), the

substrate 1 (P well region 1b) is set to have a ground potential and a voltage
is applied to the control gate electrode 8 so that a voltage is applied to the
tunnel film 5. Accordingly, an accelerated evaluation can be performed.
Further, in this test, the retention, i.e., the charge retention property is
evaluated by measuring a change in threshold voltage Vt.

Detailed Description Text - DETX (20):
Thus, the 95% retention lifetimes (time) and the field intensities of the
tunnel film 5 when Vcg=-4 V, -5 V, and -6 V can be obtained. These values are
plotted as shown in FIG. 5, thereby revealing a relation of the charge
retention lifetime with respect to the field intensity of the tunnel film 5.
The 95% retention lifetime when Vcg=0 (applied voltage is zero) is extrapolated
based on the plotted result. That is, the lifetime when the voltage applied to
the control gate electrode 8 is zero is calculated as the charge retention
lifetime at an ambient **temperature** of 125.degree. C.

Detailed Description Text - DETX (22):
Thus, the charge retention lifetime evaluation is performed on the memory by
the accelerated test in which the voltage is applied to the control gate
electrode 8 at the **temperature** (for instance, 125.degree. C.) that cannot
recover the damage, which is caused to the tunnel film 5 by the **data** rewriting,
during the charge **retention lifetime** evaluation. Accordingly, the evaluation
time can be shortened. Further, since the damages are not recovered, the
evaluation can be performed accurately when the charge retention test is
performed after rewriting data.

Detailed Description Text - DETX (24):

FIG. 6 shows a retention measurement result when no voltage is applied across the control gate electrode and the substrate. Incidentally, the ambient **temperature** in FIG. 6 is 172.degree. C. FIG. 6 corresponds to FIG. 4, and the threshold voltage is measured in an elapsed time range of approximately 7 min. to approximately 10000 min. In FIG. 6, curve L.sub.2 (indicated with a solid line) is drawn to pass through eight plotted points. Accordingly, approximately 3.times.10.sup.5 min. is extrapolated as a 95% retention lifetime.

Detailed Description Text - DETX (25):

If the 95% retention lifetime is not calculated by the extrapolation of the curve L.sub.2 passing through the plotted points but is evaluated directly, however, the evaluation requires a very long period of time, i.e., 3.times.10.sup.5 min.=approximately 6.9 months. Even if the 95% **retention lifetime** is determined by the extrapolation, approximately 10000 min. (=approximately 1 week) is required as an evaluation period of time for sampling the **data**. In addition, since the extrapolation is utilized, as indicated by chain lines L.sub.3 and L.sub.4 in FIG. 6, errors are liable to occur due to how the curve is extrapolated, resulting in a calculation error of the 95% retention lifetime.

Detailed Description Text - DETX (28):

When the charge **retention lifetime** is evaluated after rewriting **data,** accelerated evaluation is performed by intentionally applying a voltage to the tunnel film 5. Accordingly, the charge retention lifetime evaluation can be performed for a short time even at a **temperature** atmosphere where rewriting

damage to the tunnel film 5 is not recovered. Since the damage to the tunnel
film 5 is not recovered, the evaluation can be performed accurately, and for a
short time due to the acceleration by the applied voltage.

Detailed Description Text - DETX (31):
The evaluation atmosphere described above has a **temperature** of 125.degree.
C., which does not recover the damage to the tunnel film 5. However, the
temperature of the evaluation atmosphere may be further raised in a range not
recovering the damage to the tunnel film 5. Accordingly, the period of time
can be further shortened by raising the **temperature** more in the range not
recovering the damages of the tunnel film 5, as compared to that at the lower
temperature in the same range.

Detailed Description Text - DETX (32):
Further, in the above explanation, although the charge **retention lifetime** is
evaluated after rewriting **data,** the charge **retention lifetime** may be evaluated
without rewriting **data**. In this case, the period of time for evaluating the
charge retention lifetime can be further shortened, and the evaluation ambient
temperature is arbitrary. The present invention can be applied to various
nonvolatile semiconductor memories such as an EEPROM, an EPROM, and an MNOS
memory, in addition to the flash memory.

Claims Text - CLTX (18):
10. The charge **retention lifetime** evaluation method of claim 1, wherein the
charge **retention lifetime** is evaluated after writing, erasing, and rewriting of
data are performed to the nonvolatile semiconductor memory.

Claims Text - CLTX (19):

11. The charge **retention lifetime** evaluation method of claim 1, further comprising writing **data** into the nonvolatile semiconductor device so that damages are caused to the tunnel film, before evaluating the charge **retention lifetime,**

Claims Text - CLTX (20):
wherein the tunnel film voltage is applied to the tunnel film at a **temperature** lower than a **temperature** capable of recovering the damages.

Claims Text - CLTX (21):
12. The charge retention lifetime evaluation method of claim 11, wherein the tunnel film voltage is applied to the tunnel film at the **temperature** equal to or higher than 125.degree. C.

Claims Text - CLTX (22):
13. The charge retention lifetime evaluation method of claim 1, wherein the tunnel film voltage is applied to the tunnel film in an operational **temperature** range where the nonvolatile semiconductor memory is practically used.

Claims Text - CLTX (23):
14. The charge retention lifetime evaluation method of claim 13, wherein the tunnel film voltage is applied to the tunnel film at a maximum **temperature** in the operational **temperature** range where the nonvolatile semiconductor memory is practically used.

Claims Text - CLTX (30):
estimating a charge **retention lifetime** of the written **data** when a third voltage smaller than the first and second voltages is externally applied to the

tunnel film, by the first and second charge **retention** properties.

Claims Text - CLTX (42):
23. The charge retention lifetime evaluation method of claim 16, wherein
the first and second voltages are respectively applied at temperatures in an
operational **temperature** range at which the nonvolatile semiconductor memory is
practically used, to evaluate the first and second charge retention properties.

Claims Text - CLTX (43):
24. The charge retention lifetime evaluation method of claim 23, wherein
the first and second voltages are respectively applied at a maximum **temperature**
in the operational **temperature** range at which the nonvolatile semiconductor
memory is practically used.

Claims Text - CLTX (44):
25. The charge retention lifetime evaluation method of claim 23, wherein
the first and second voltages are applied at a same **temperature**.

Claims Text - CLTX (48):
29. The charge **retention lifetime** evaluation method of claim 27, wherein
the first and second temperatures are lower than a **temperature** capable of
recovering damages to the tunnel film produced when the **data** is written into
the nonvolatile semiconductor memory.

US-PAT-NO: 6232153

DOCUMENT-IDENTIFIER: US 6232153 B1

TITLE: Plastic package assembly method for a ferroelectric-based integrated circuit

---------- KWIC ---------

Abstract Text - ABTX (1):

A plastic package assembly method suitable for ferroelectric-based integrated circuits includes a strict thermal budget that reduces the time at **temperature** for four key processing steps: die attach cures, die coat cures, molding cures, and marking cures. The plastic package assembly method uses low **temperature** mold and die coat materials, as well as low **temperature** curable inks or laser marking in order to minimize degradation of electrical performance, thus improving yields and reliability. The assembly method uses a snap cure die attach step, a die coat followed by a room **temperature** cure, and formation of the plastic package with room **temperature** curable molding compounds not requiring a post mold cure. Front and back marking of the plastic package is accomplished using either an infrared or ultraviolet curable ink followed by minimum cure time at elevated **temperature,** or by using laser marking.

Brief Summary Text - BSTX (3):

Ferroelectric memory products generally exhibit poor performance in plastic packages as compared to other packaging options such as ceramic packages. One

of the chief causes of the poor performance is the elevated temperatures that the ferroelectric integrated circuit is exposed to for extended times during plastic package assembly. Typically, combined cures performed during plastic package assembly of ferroelectric memories can be as long as ten hours at temperatures that can activate undesirable imprint mechanisms as these temperatures approach the Curie point of the ferroelectric dielectric material used. Current assembly methods use ink cures, wafer mount cures, die attach cures, wire bonding, die coat cures, molding, molding cures, as well as back and top marking cures. Each of these processing steps contribute to the time spent at an elevated **temperature,** which can adversely affect electrical performance.

Brief Summary Text - BSTX (4):

A typical prior art plastic package assembly flow 10 is shown in FIG. 1. Note that not every plastic package assembly step is shown in FIG. 1, only those steps having a significant "time at **temperature**" exposure, and that are significantly altered in the plastic packaging method of the present invention, which is described in further detail below.

Brief Summary Text - BSTX (5):

A typical die attach step 12 is referenced in FIG. 1, which is usually performed at a **temperature** of 175.degree. C. or more for at least an hour. A typical die coat and curing step 14 is referenced in FIG. 1, which is usually performed at a **temperature** of 150.degree. C. or more for at least two hours. After the plastic package is formed during a molding step, a typical post mold curing step 16 is referenced in FIG. 1, which can be performed at a **temperature**

of 175.degree. C. or more for at least five hours. After the package is
inked, a typical back mark curing step 18 is referenced in FIG. 1, which can be
performed at a **temperature** of 175.degree. C. or more for at least two hours.
A typical front or top mark curing step 20 is referenced in FIG. 1, which can
be performed at a **temperature** of 175.degree. C. or more for at least two
hours.

Brief Summary Text - BSTX (6):

The adverse effects of time spent at **temperature** for ferroelectric devices
can be further analyzed with respect to a hysteresis loop, which is a
representation of the charge versus voltage characteristics of a ferroelectric
device. A typical hysteresis loop 22 for a ferroelectric capacitor is shown in
FIG. 2. The size and shape of hysteresis loop 22 can be used to characterize
the electrical performance of a ferroelectric capacitor, and can also be used
to diagnose the degradation of electrical performance due to exposure at
elevated temperatures for extended times. Data retention reliability can be
adversely affected by changes in the ferroelectric capacitor due to exposure of
the integrated circuit at elevated temperatures for extended times. Switched
charge (Q.sub.sw) loss due to thermal depolarization at elevated temperatures
approaching, but not exceeding, the Curie point affect the retention
performance of the completely fabricated, plastic packaged ferroelectric
memory. Asymmetry, which is the undesirable shift in hysteresis loop 22 along
the voltage (X) axis, is also impacted as a result of extended times at
elevated temperatures. With reference to the P, U, N, and D charge components
associated with hysteresis loop 22 of FIG. 2, switched charge and asymmetry are

defined as follows:

Brief Summary Text - BSTX (12):
According to the present invention, a "ferroelectric friendly" plastic package assembly method includes a strict thermal budget that reduces the time at **temperature** for four key processing steps: die attach cures, die coat cures, molding cures, and marking cures, while still providing a suitable plastic package for a ferroelectric-based integrated circuit. The plastic package assembly method of the present invention uses low **temperature** mold and die coat materials, as well as low **temperature** curable inks or laser marking in order to minimize degradation of electrical performance, thus improving manufacturing yields and reliability.

Brief Summary Text - BSTX (13):
In part, the method of the present invention uses a snap cure die attach step, a die coat followed by a room **temperature** cure, and forming the plastic package with room **temperature** curable molding compounds not requiring a post mold cure. Top and back marking of the plastic package is accomplished using an infrared ink followed by minimum cure time at elevated **temperature,** by using laser marking, or by using ultraviolet curable ink.

Detailed Description Text - DETX (2):
Referring now to FIG. 3, a "ferroelectric friendly" plastic package flow 30 is shown according to the present invention. It is important to note that not all of the many manufacturing steps commonly found in plastic packing are shown in the flow chart of FIG. 3. Steps like die bonding and inking of the tested integrated circuits at the wafer level are well known to those skilled in the

art and need not be unnecessarily repeated. Further, the time and **temperature** profile of these many steps are not especially damaging to the electrical performance of the ferroelectric memory or integrated circuit and therefore these steps are not materially altered according to the method of the present invention. Only those steps shown and described in further detail with respect to FIG. 3 have been materially altered in order to change the time and **temperature** profile.

Detailed Description Text - DETX (4):

Referring to FIG. 3, the first step 32 is the die attach step in which the integrated circuit die such as a ferroelectric memory chip is attached to a conventional lead frame. Die attach step 32 is performed using a "snap cure" in which the die attach compound is instantly cured by a momentary exposure (one minute or less) to an elevated **temperature**. The snap cure used in the method of the present invention is done using a seven zone tunnel die attach heater block set at temperatures of 170, 180, 200, 200, 200, 190, and 180.degree. C. The units pass through the tunnel via a conveyer belt and take a total of about one minute to pass through the tunnel. The die attach compound used is a gold-filled epoxy such as compound CRM-1064 manufactured by the Sumitomo Co., Ltd. of Osaka, Japan.

Detailed Description Text - DETX (5):

Referring now to FIG. 4, the yield improvement results at the die attach step 32 (with respect to the conventional die attach described above in the Background of the Invention) for both short term and long term memory retention are shown. Short term memory retention is defined as maintaining a memory

state for four hours at 150.degree. C. Short term memory retention testing is a retention test typically conducted during production testing to screen out infant failures. Long term memory retention is defined as maintaining a memory state for 72 hours at 150.degree. C. Long term **memory retention** testing is a **retention** test used to measure the median **lifetime** of the product under test and is an indicator of long term reliability in terms of **data retention**. Referring again to FIG. 4, while short term memory retention is only marginally improved, long term retention is improved by a factor of about 2.8.

Detailed Description Text - DETX (7):

Referring again to FIG. 3, the second step 34 is the die coating and curing step in which the ferroelectric integrated circuit die, which is attached to the lead frame, is conformally coated with a suitable die coating material. The die coating step 32 is performed at room **temperature**. The coated die is cured at room **temperature,** with typical curing times ranging between 12 and 24 hours, although other curing times can be used depending upon the die coating material selected. The die coating material used is a soft transparent silicone encapsulant such as coating material Hipec Q3-6633 manufactured by the Dow Corning Corporation of Midland, Mich. Silicone-based coating materials should be mixed in two-to-one or other ratios as specified by the vendor.

Detailed Description Text - DETX (10):

Referring again to FIG. 3, in forming the plastic package, a room **temperature** molding compound is used that does not require a separate postmold curing step. In other words, the plastic package is complete and essentially

ready for further processing steps as it is released from the mold. The total time at **temperature** inside of the mold required to form the plastic package is about one minute at 175.degree. C. A block 36 referencing the lack of a separate post mold cure at elevated temperatures is shown in FIG. 3. The molding compound used is a plastic epoxy such as molding compound 6600R manufactured by the Sumitomo Co., Ltd. of Osaka, Japan.

Detailed Description Text - DETX (13):

As explained earlier, the marking steps in which the front and back surfaces of the plastic package are marked with symbols such as trademarks, identifying numerals and the like, can be a significant source of time at elevated **temperature,** and thus contributes to degradation of electrical performance in ferroelectric-based memories and integrated circuits. Accordingly, the method of the present invention offers three low **temperature** alternatives for marking: inking followed by an infrared cure; inking followed by an ultraviolet cure; and laser marking.

Detailed Description Text - DETX (14):

Heat-cure (infrared) marking can be used since it provides good contrast, exceptionally good mark permanency and overall good quality of marking. It is usable with various molding compounds, including the room **temperature** molding compound referred to above, without much variation in quality. Steps 38 and 44 shown in FIG. 3 are the back mark and front mark cure steps, respectively. After the package has been inked, the plastic package is "flash cured" by an infrared method at **temperature** ranges of between 150.degree. C. and 250.degree. C. for between 15 and 30 seconds. This is then followed by an

oven cure at 145.degree. C. to 155.degree. C. for between 1.5 and two hours.
The flash cure time and the subsequent oven cure can vary depending upon the
exact specifications provided by the ink vendor. A suitable white ink is
TPC261 manufactured by Teca-Print AG of Thayngen, Switzerland for use with the
Teca TPX350 marking machine. Another example of a suitable infrared-curable
ink is the Markem 4489 ink manufactured by the Markem Corporation of Keene,
N.H.

Detailed Description Text - DETX (19):
The results for the entire **temperature**-optimized assembly flow 30 of the
present invention is shown with respect to FIGS. 12 and 13, using any of the
three marking options. Significant yield improvements and reduction in failing
bits were achieved due to the strict time-**temperature** budget required by the
assembly method of the present invention.

Detailed Description Text - DETX (22):
In conclusion, the plastic package assembly method of the present invention
significantly improves both the yield and reliability of a ferroelectric-based
integrated circuit such as a ferroelectric memory circuit when compared to the
electrical performance of the same circuits when plastic-packaged using prior
art techniques requiring extended times at elevated temperatures. In the
method of the present invention, if infrared marking is used, the time at
elevated temperatures above 145.degree. C. is between about 1.5 and 2 hours.
If either laser marking or ultraviolet-curable inks are used in marking, the
time at the same elevated **temperature** can be reduced to three minutes or less.

Claims Text - CLTX (7):
curing the marked surface of the plastic package, such that the total time
the ferroelectric integrated circuit is exposed to a **temperature** of above
145.degree. C. is at most two hours and the short term memory retention is
improved by a factor of at least 1.9 when compared with a conventional assembly
method involving more than two hours at a **temperature** above 145.degree. C.

Claims Text - CLTX (8):
2. The plastic package assembly method of claim 1 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
about 1.5 hours.

Claims Text - CLTX (9):
3. The plastic package assembly method of claim 1 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
about three minutes.

Claims Text - CLTX (16):
curing the marked surface of the plastic package, such that the total time
the ferroelectric integrated circuit is exposed to a **temperature** of above
145.degree. C. is at most two hours and the long term memory retention is
improved by a factor of at least 2.8 when compared to a conventional assembly
method involving more than two hours at a **temperature** above 145.degree. C.

Claims Text - CLTX (17):
5. The plastic package assembly method of claim 4 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
at most 1.5 hours.

Claims Text - CLTX (18):
6. The plastic package assembly method of claim 4 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
about 3 minutes.

Claims Text - CLTX (25):
curing the marked surface of the plastic package, such that the total time
the ferroelectric integrated circuit is exposed to a **temperature** of above
145.degree. C. is at most two hours and the number of failing bits is reduced
by a factor of at least 135 for short term memory retention when compared to a
conventional assembly method involving more than two hours at a **temperature**
above 145.degree. C.

Claims Text - CLTX (26):
8. The plastic package assembly method of claim 7 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
at most 1.5 hours.

Claims Text - CLTX (27):
9. The plastic package assembly method of claim 7 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
about 3 minutes.

Claims Text - CLTX (34):
curing the marked surface of the plastic package, such that the total time
the ferroelectric integrated circuit is exposed to a **temperature** of above
145.degree. C. is at most two hours and the number of failing bits is reduced
by a factor of at least 113 for long term memory retention

when compared to a
conventional assembly method involving more than two hours
at a **temperature**
above 145.degree. C.

Claims Text - CLTX (35):
11. The plastic package assembly method of claim 10 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
at most 1.5 hours.

Claims Text - CLTX (36):
12. The plastic package assembly method of claim 10 in which the total time
the integrated circuit is exposed to a **temperature** of above 145.degree. C. is
about 3 minutes.